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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/428,052	10/27/1999	KIYOSHI IRINO	970901A	4139

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WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP  
1250 CONNECTICUT AVENUE, NW  
SUITE 700  
WASHINGTON, DC 20036

EXAMINER
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DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/428,052	Applicant(s) IRINO, KIYOSHI	
	Examiner José R Díaz	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 08 December 2003.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 6, 10 and 15-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 6, 10 and 15-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☒ Certified copies of the priority documents have been received in Application No. 08/917,936.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 8, 2003 has been entered.

### ***Allowable Subject Matter***

The indicated allowability of claims 6, 15 and 16 is withdrawn in view of the newly discovered reference to Wristers et al. (US Pat. No. 5,674,788). Rejections based on the newly cited reference follow.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

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the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (US Pat. No. 5,650,344, which is the parent case of the previously cited reference U.S. 5,808,348) in view of Wristers et al. (US Pat. No. 5,674,788).

Regarding claims 6, 15 and 16, Ito et al. teaches a method of fabricating a semiconductor device, comprising the steps of: forming a gate oxide film (12) on a substrate (10) (see fig. 1B) by a thermal oxide film (see col. 1, lines 25-26); forming a gate electrode pattern (20) on said gate oxide film (see fig. 1D); forming diffusion regions electrode pattern (28, 30) in said substrate at both lateral sides of said gate electrode pattern by introducing an impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask (see fig. 1E and col. 4, lines 36-38); introducing N atoms (22) into said gate oxide film (see fig. 1D) while using said gate electrode pattern a mask (see col. 3, lines 36-41); depositing, after said step of introducing N atoms, a CVD-oxide film (32) on said gate oxide film by a CVD process (see fig. 3 and col. 4, lines 47-50), wherein said step of introducing said impurity element being conducted prior to said step of introducing N atoms into said gate oxide film (see col. 5, lines 55-57), wherein said step of introducing N atoms into said gate

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oxide film comprises a thermal annealing process of said gate oxide film (see col. 3, lines 36-41), wherein activation of said impurity element is conducted simultaneously to said thermal annealing process (see col. 4, lines 45-47).

However, Ito et al. fails to teach the following limitation: a thermal annealing process of said gate oxide film conducted in an atmosphere containing NO, wherein said thermal annealing process being conducted at a temperature of about 800°C. Wristers et al. teaches a very well known nitridation process conducted in an atmosphere containing NO and at a temperature of about 800°C (see col. 3, lines 53-55-25, col. 5, lines 29-36, and col. 7, lines 4-8).

Ito et al. and Wristers et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a nitridation process conducted in an atmosphere containing NO and at a temperature of about 800°C. The motivation for doing so, as is taught by Wristers et al., is reducing the number of high-energy electrons (i.e. hot electrons) injected into and thereafter trapped within the gate dielectric (col. 4, lines 47-49). Therefore, it would have been obvious to combine Wristers et al. with Ito et al. to obtain the invention of claims 6, 15 and 16.

Claims 10, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Duane (US Pat. No. 5,804,496).

Regarding claim 10, Duane teaches a method of fabricating a semiconductor device, comprising the steps of: forming a gate oxide film (203) on a substrate (201)

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(see fig. 2A) by a thermal oxide film (see col. 3, lines 8-9); forming a gate electrode pattern (205) on said gate oxide film (203) such that said gate electrode pattern is in direct contact with said oxide film (see fig. 2A); forming diffusion regions (213) in said substrate at both lateral sides of said gate electrode pattern by introducing impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask (see fig. 2B); and introducing N atoms (219) (see fig. 2C), after said step of introducing said impurity element (see fig. 2C), into said gate oxide film (203) while using said gate electrode pattern as a mask (see col. 5, lines 6-8), such that said N atoms do not reach said substrate (see col. 5, lines 1-6), wherein said step of introducing N atoms into said gate oxide film includes an ion implantation process of N ions (see col. 4, lines 54-55) conducted with a dose of  $1 - 3 \times 10^{14} \text{ cm}^2$  (see col. 4, line 56). In addition, Duane teaches that the ion implantation process can be made at energy levels where no edge dopant (e.g. N atoms) penetrates the active region (see fig. 5, lines 1-3). Therefore, it would have been obvious to one of ordinary skill in the art to conduct the ion implantation at an acceleration voltage not exceeding 10keV, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 17, Duane teaches that the ion implantation process is conducted such that N ions are introduced perpendicularly (i.e.  $90^\circ$ ) to said gate oxide film (see col. 3, lines 65-67).

Regarding claim 18, Duane teaches that some of said N atoms are incorporated into gate oxide film (see col. 5, lines 6-7). Therefore, it would have been obvious to one

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of ordinary skill in the art to incorporated N atoms into the gate oxide at a concentration of 0.5-3%, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Huang*, 40 USPQ2d 1685,1688(Fed. Cir. 1996) citing *In re Aller*, 105 USPQ 233, 235 (CCPA 1955).

### ***Response to Arguments***

Applicant's arguments with respect to claims 6, 10, and 15-18 have been considered but are moot in view of the new grounds of rejection.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kuroi et al. (US Pat. No. 6,232,187 B1) discloses different the step of incorporating nitrogen into the gate oxide layer by annealing in NO (col. 10, lines 5) and/or ion implantation (col. 11, lines 8-23).

### ***Correspondence***

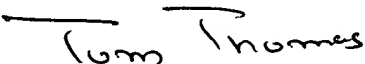
Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on 9:00-5:00 Monday through Friday.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD  
3/9/04

  
Tom Thomas  
Supervisory Patent Examiner  
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